Effect of Commutation inductor in ZVS and clamped voltage

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Abstract-This paper presents an analysis of the effect of commutation inductor in ZVS and clamped voltage. To construct such converters, a switch cell, which consists of the basic PWM switch cell and an additional commutation inductor circuit, is proposed. Using this switch cell, a family of single-switch ZVS-CV converter topologies can be derived. These converters have the reduction of turn-on loss and noise, and the minimum voltage stress across the switch. As an example, the operating principle and the steady-state analysis for Cuk and boost converters are described and are verified experimentally.

1.INTRODUCTION

Zero-voltage-switched (ZVS) resonant converters utilizing soft-switching techniques can operate at higher switching frequency than the hard-switched PWM converters. In recent years, a number of ZVS resonant converters have been proposed. The resonant converter topologies, which utilize the resonant transition, are generated by addition of resonant elements to the conventional PWM converters. However, in these resonant converters much higher voltage stress arises across the switch due to the resonant manner. Therefore these converters inevitably require high-voltage-rating devices, which results in an increasing conduction loss. On the other hand, a new soft-switching technique to remedy this drawback has recently been proposed. Those converters are called "Zero-voltage-switching and clamped voltage (ZVS-CV) type converters." In general, ZVS-CV converters usually need two active switches and a few additional resonant elements because a resonant transition during the off interval of both switches is required and the voltage regulation is performed by the constant-switching-frequency PWM controller. Unlike the above method, an attractive realization of the ZVS-CV type converter which uses only one active switch and one diode has been proposed, where the output filter inductor is used as a resonant element and so the ripple voltage due to ESR of the output capacitor becomes large.

In this paper, an alternative topology of ZVS-CV converters using one active switch and one diode is presented, where a concept of switch cell is introduced. This switch cell is generated by addition of a commutation inductor circuit, which is a series connection of a resonant inductor and a relatively large capacitor, into the conventional switch cell. Applying this switch cell to the conventional PWM converter (buck, boost, buck boost, and Cuk etc.), a family of single switch ZVS-CV converters can be derived. The proposed converter has a quite simple circuit configuration and the reduction of transistor turn-on loss and noise without increasing the voltage stress. However, the switching frequency variation is required to regulate the output voltage of the converter. This paper presents the operating principle and the analytical expressions of steady-state characteristics for Cuk and boost type ZVS-CV converters. Furthermore the analysis is verified by comparing with the experimental results.

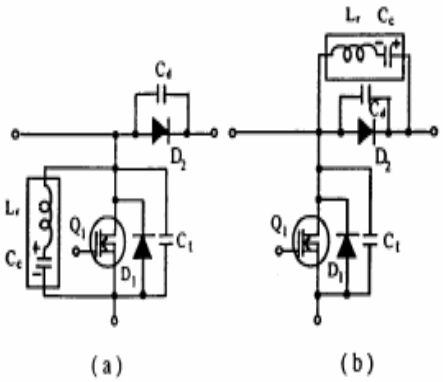


Fig.1 ZVS-CV switch cell.

2. PRINCIPLE OF ZVS-CV

Switch cell configurations for ZVS-CV operation are shown in Fig.1. In these switch cells, a series circuit of commutation inductor Lr and large capacitor Cc is added across the transistor or diode. ZVS-CV dc-dc converters can be constructed by replacing either switch cell of Fig.I(a) or (b) with that of the conventional PWM converters. These
switch cells are composed of the conventional switch cell and a series circuit of commutation inductor and large capacitor Cc. The commutation inductor Lr forms a resonant circuit with two parasitic capacitances of transistor Q_1 and diode D_2 while both switches are off state. In most cases, external capacitors are added in parallel with these capacitances. The commutation inductor current is used for charging and discharging the capacitances C_t and C_d during the resonant transition. The capacitor Cc in series with Lr is used for blocking a dc current flowing through the commutation inductor circuit.

ZVS-CV operating principle is as follows: First, consider the time when the transistor is turned off. At this time, the diode also remains off state, and so both transistor and diode are off state. The parallel capacitors of Q_1 and D_2 resonate with b, and the capacitors C_t and C_d are charged and discharged, respectively. When the capacitor Ct is completely charged, D2 conducts and the transistor voltage is clamped. Then the former resonant transition finishes. Next, the commutation inductor current continues to flow through diode D2, and decreases linearly. When this forward current of D_2 becomes zero, D_2 turns off. Thus both transistor Q_1 and diode D_2 are off state again. The capacitor C_t of transistor is discharged and the capacitor Cd of diode D_2 is charged owing to the commutation inductor current which flows in the direction opposite to the former

resonance. With this action, the transistor voltage gradually decreases until it reaches zero and its anti parallel diode D_1 conducts, i.e. the latter resonant transition finishes. To achieve the ZVS operation, transistor Q_1 has to be turned on during the conduction of D_1.The voltage conversion ratio for ZVS operation in limited. Detailed analyses are discussed in the next section.

3. ANALYSIS OF ZVS-CV CUK CONVERTER

3. 1 Expressions for Operation Stages.

The first discussion is on ZVS-CV Cuk converter shown in Fig.2. The key switching waveforms of this converter are shown in Fig.3, where one switching cycle starts with the turn-off action of transistor Q_1 and there are four different stages. The equivalent circuits corresponding to each stage are shown in Fig.4. To simplify the analysis, the input and output filter currents Ii and Io are assumed to be a constant current sources, and the voltage V_1 of energy transferring capacitor and the output voltage V_o are also assumed to be a constant voltage sources.

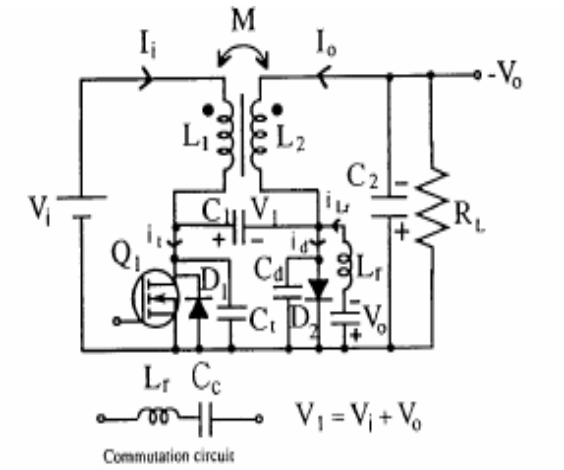


Fig.2 ZVS-CV Cuk converter.

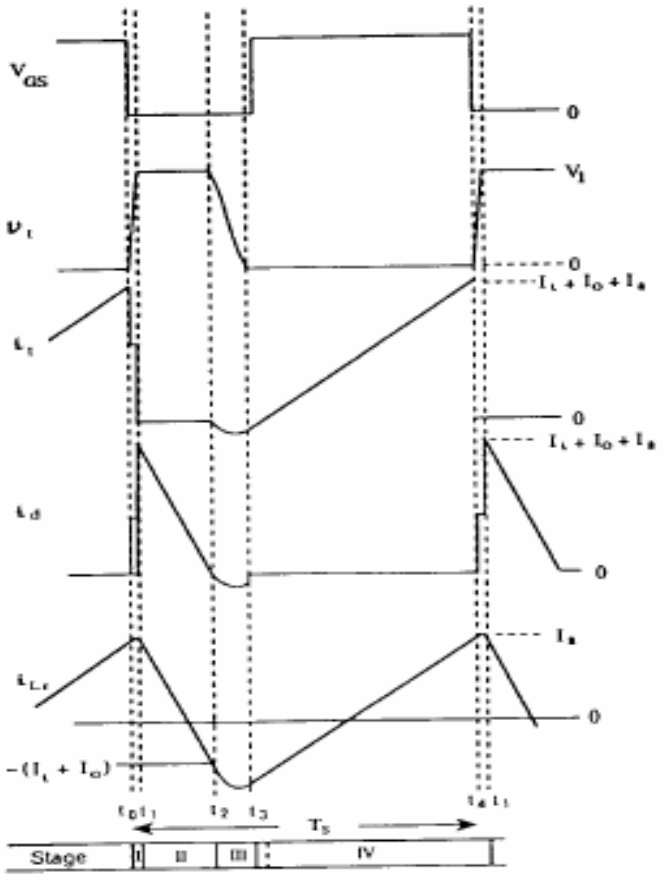


Fig.3 Waveforms of ZVS-CV Cuk converter.

Before going into the analysis, the following parameters are defined:

characteristic impedance :

$Z_n = \sqrt{\{Lr/(C_t+C_d)\}}$

resonant angular frequency :

$Wr = 2\Pi f = 1 / \sqrt{(C_t+C_d)}$

voltage conversion ratio : $x = V_o/V_i$

normalized switching frequency :

$F = fs / fr$

normalized load resistance: $r = R_L / Z_n$

The circuit operation of ZVS-CV Cuk converter is described as follows:

Stage I ($T_{01}=t_1-t_0$):
During this stage, the converter is represented by the equivalent circuit shown in Fig.4(a), where both transistor Q1 and diode D2 are off. The commutation inductor Lr capacitors C_t

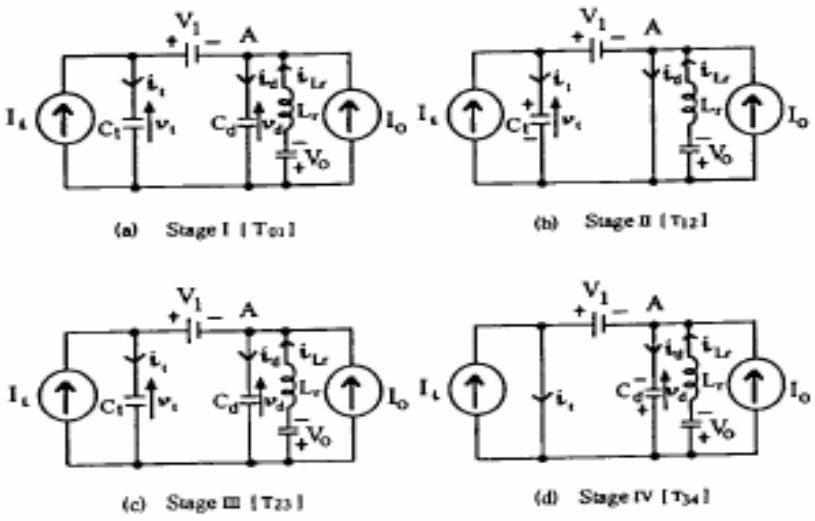


Fig.4 Equivalent circuits for four operation stages of ZVS-CV Cuk converter.

and C_d constitute a resonant circuit. The input and output currents and the commutation inductor current are related to the charge of C, and the discharge of C_d. From the equivalent circuit, the state equations for this stage are expressed as

$I_i+I_0=-i_{LR}+C_r (dv_t/dt)+C_d (dv_d/dt)$ (1)

$V_0=-Lr (di_{LR}/dt)- v_d$ (2)

$V_1=v_t - v_d$ (3)

with the initial conditions

$v_d (0)=-V_1$, $i_{LR} (0)=Ia$ (4)

where Ia, is the approximate peak value of commutation inductor current. Solving the above differential equations, the time functions of inductor current and transistor voltage are obtained as

$i_{LR} (t) = - I_i + I_0 + \sqrt{[(Vi/Zn)^2+(I_i+I_0+Ia)]}$

$\sin(Wr\, t+ \theta)$ (5)

$v_t (t)=Vi -\sqrt{[(Vi)^2+\{Zn(I_i+I_0+Ia)\}^2]}$

$\cos(Wr\, t+ \theta)$ (6)

Where $\theta=\tan^{-1}[Zn(I_i+I_0+Ia)/Vi]$ (7)

When the transistor voltage V_t exceeds $V_1=(=V_i+V_o)$ at time ti, diode D_2 is forward-biased and tums on. As a result, transistor Q_1 goes into a voltage clamping mode, which is the second stage. Therefore the interval of this resonant stage is

$t_{01}=\{(Ct+Cd)(Vi+Vo)\}/ (I_i+I_0+Ia)$ (8)

Stage II ($T_{12}=t_2-t_1$) :
In this stage, the voltage across Q1 is clamped at voltage V_i. From the equivalent circuit shown in Fig.4(b), the state equations are as follows:

$i_i = - i_{LR} + i_d$ (9)

$V_0 = -Lr (di_{LR}/dt)$ (10)

with the initial conditions $i_{LR} (0)=Ia$ (11)

The solution of the above equations is expressed as

$i_{LR}(t)=Ia-(Vo/Lr)t$ (12)

$i_d(t)= I_i+I_0+Ia-(Vo/Lr)t$ (13)

The commutation inductor current flows through diode D_2.and decreases linearity as shown in Fig.3. Therefore diode current id also decreases. Finally it reaches zero at time t_2, and diode D_2 tums off. The time interval of this stage is

$T_{12}=\{L_r (I_i+I_0+Ia)\}/V_o$ (14)

Stage III ($T_{23} = t_3-t_2$):
In this interval, both transistor Q_1 and diode D_2 are off state. ***So*** the resonant circuit composed of Lr**,** Ct, and Cd operates again. From the equivalent circuit shown in
Fig4(c), the state equations for this stage are

$I_i+I_0= - i_{LR} +Ct (dV_t/dt)+Cd(dV_d/dt)$ (15)

$Vo=-Lr (di_{LR}/dt)-V_d$ (16)

$V_1=V_t-V_d$ (17)

with initial conditions

$Vt(o)=V_1$, $V_d(0)=0$,

$i_{LR}(0)= - (I_i+I_0)$ (18)

The solution is as follows:

$V_t(t)=V_i+V_o \cos W_r t$ (19)

$i_{LR}(t)=-(Ii+Io)-(Vo/Zn) \sin W_r t$ (20)

In this stage, the commutation inductor current flows in the direction opposite to stage I and its amplitude exceeds the sum of input and output currents. Then the capacitor C_t is
discharged and the transistor voltage gradually decreases until it reaches zero and the stage changes into Stage **IV.** Therefore the time interval T_{23} of this stage is obtained from

$V_t(T_{23})=(Vi+Vo)\cos w_r T23=0$ (21)

As a result we have

$T_{23}=\alpha/W_r$ (22)

Where $\alpha=\cos^{-1}(-V_i/V_o)$ (23)

Furthermore this discussion derives the **ZVS** condition. To maintain **ZVS** operation, the existence of T23 is required. i.e.. the condition **Vo** $\geq$ **Vi** is obtained from (21). This equation is rewritten as

x ≥ 1 (24)

Stage 1V ($T_{34}=t_4-t_3$):
At the beginning of this stage, the transistor current flows through the anti parallel diode of Q1. During this short time, transistor Q1 has to be turned on. From the equivalent
circuit shown in Fig.4(d), the state equation for this stage is

$V_i=Lr(d\, i_{LR}/dt)$ (25)

with the initial condition

$i_{LR}(0)=-(Ii+Io)-(V_o/Z_n)\sin\alpha$ (26)

The solution is

$$i_{LR}(t)=-(Ii+Io)-(V_o/Z_n)\sin\alpha+(V_i/L_r)t \quad (27)$$

The interval T34 of this stage is varied to control the output voltage. It is assumed that Stage I in the next cycle begins when the commutation inductor current iLr reaches I,.
Therefore the time interval T34 is expressed as

$$T_{34}=[L_r\{I_a+Ii+Io+(Vo/Zn)\sin\alpha\}]/Vi \quad (28)$$

By summing each interval of the above four stages, one switching period Ts is expressed as

$$Ts=T_{O1}+T_{I2}+T_{23}+T_{34} \quad (29)$$

To obtain the dc voltage conversion ratio of ZVS-CV Cuk converter, let us consider the sum of average currents flowing into node **A** in Fig. 4, i.e.

$$(I_i-i_t)-i_d+i_{LR}+I_0=0 \quad (30)$$

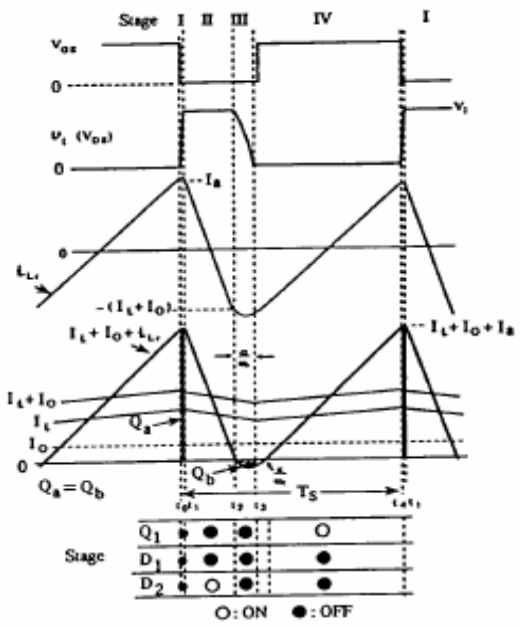


Fig.5 Relation beetween input and output currents I_i , I_o, and commutation inductor current i_{Lr} in ZVS-CV Cuk converter.

The first term is the average current flowing through the capacitor **C_1.** It is zero because the capacitor C1 is assumed to be a constant voltage source **V_1**. The third term, i.e. the
average value of inductor current i_{LR} is also zero.
Furthermore, the voltage across the output diode is clamped at a constant voltage **$-V_1$,** during Stage **IV,** and so its current does not flow. Hence the fourth term is zero. Therefore the output current is expressed as

$$I_o=\{(Ii+Ia+i_o)T_{12}\}/(2T_S) \quad (31)$$

Substituting (14) into (31) and using Vo = $R_L I_o$, the following equation related to the current (Ii + i_o + Ia) is found as

$$(Ii+i_o+Ia=\sqrt{\{(2Ts)/Lr\,R_L)\}}\,V_o \quad (32)$$

4. ANALYSIS OF ZVS-CV BOOST CONVERTER

The above mentioned analytical procedure is applicable for the ZVS-CV boost converter shown in Fig.6. The key switching waveforms of this converter are shown in Fig.7. As seen in this figure, there are four stages during one switching period**.** The equivalent circuits of each stage of this converter are shown in fig.8. The analysis of ZVS-CV boost converter is almost similar to that of ZVS-CV Cuk converter.

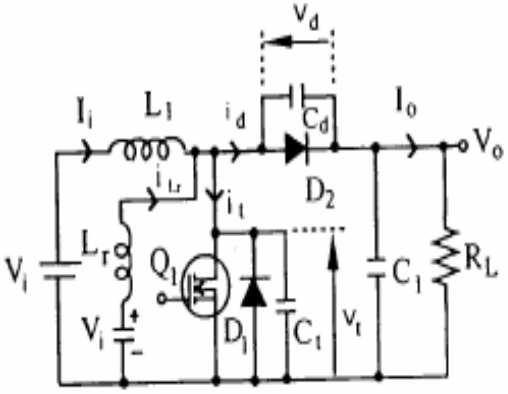


Fig.6 ZVS-CV boost converter.

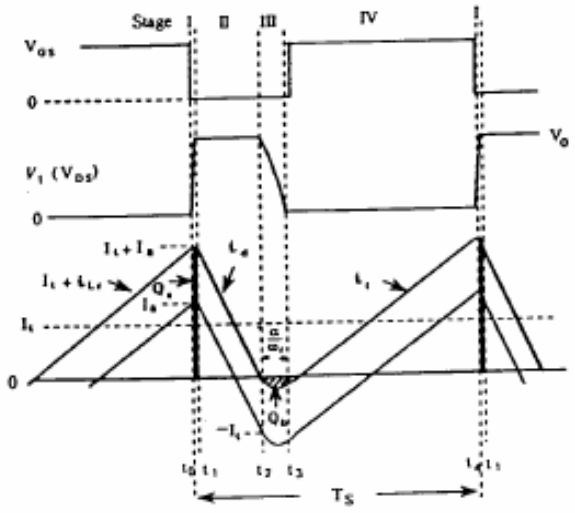


Fig. 7 Waveforms of ZVS-CV boost converter.

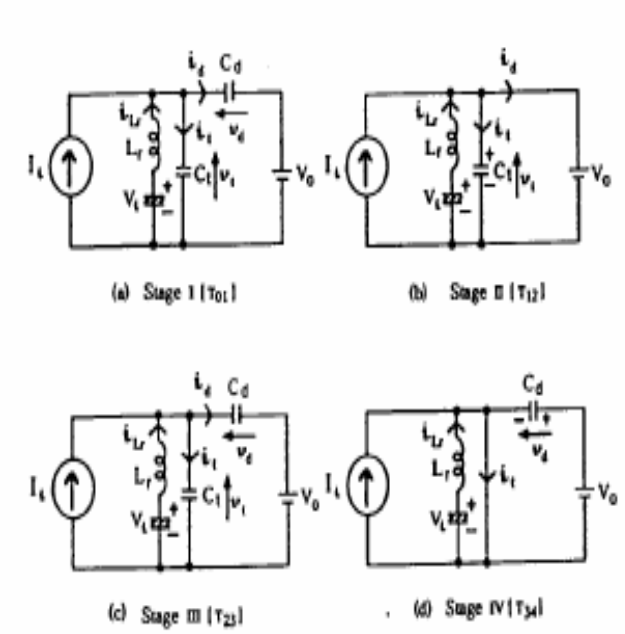
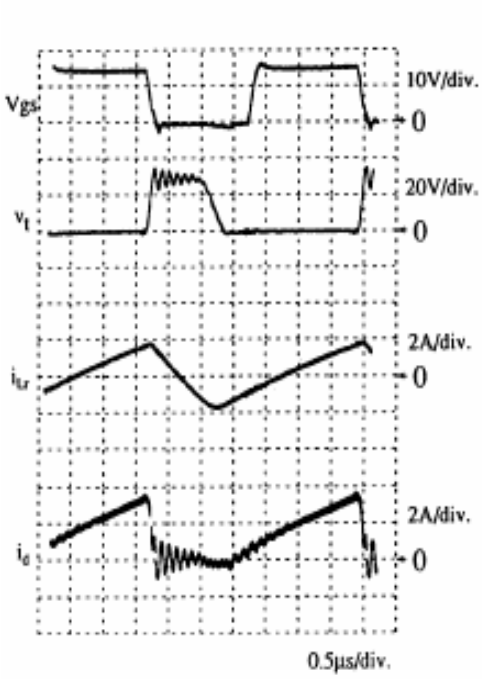


Fig.8 Equivalent circuits for four operation stages of ZVS-CV boost converter.

5. EXPERIMENTAL CONFIRMATION

To confirm the validity of the analysis described above, ZVS-CV Cuk and boost converters were implemented. IRF640 MOSFET and ESA85-009 Schottky diode were used as switching devices. Figure 9 shows experimental waveforms of ZVS-CV Cuk converter. From this figure, it is seen that the transistor tum-on noise is sufficiently suppressed but the turn-off noise remains. The turn-off noise is due to parasitic inductances associated with capacitors and lead wires. In addition, the waveforms of the primary and secondary voltages of the coupled-inductor are almost the same, and therefore the coupled-inductor property which results in a zero-current ripple at either input port or output port of the converter. Next, Figures 10 and 11 compare the analytical and experimental results on the load characteristics, and the control

characteristics, respectively. These comparisons verify the validity of the analysis. From the above results, it is clarified that the characteristics of ZVSCV converters are similar to the voltage-mode half-wave quasi-resonant converters. However, the ZVS limitation is contrary and the ZVS-CV converter has the limit of ZVS operation in the region of heavy load. Furthermore, the steady-state characteristics of the ZVS boost converters are shown in Fig.s 12 and 13, where the analysis is also confirmed experimentally.



MOSFET : IRF640 , D_1 : ESA85-009
V_i = 9 [v] , V_o = -19.5 [v] , f_s = 300 [kHz]
R_L = 60 [Ω] , I_i = 1.09 [A] , I_o = 0.35 [A]
L_1 = 370 [μH] , L_2 = 103 [μH]
L_r = 5.5 [μH] , C_1 = 3.3 [nF]
C_d = 4.7 [nF] , C_c = 47 [μF]
C_1 = 100 [μF] , C_2 = 100 [μF]

Fig.9 Experimental waveforms of ZVS-CV Cuk converter.

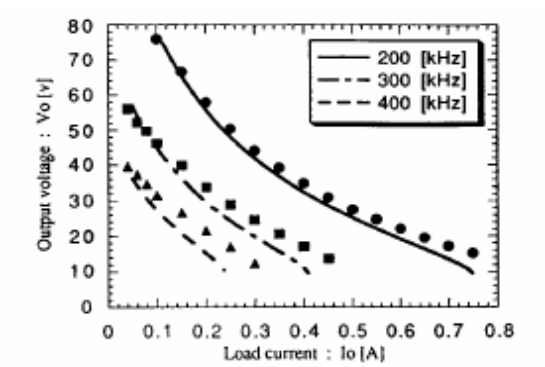


Fig.10 Load chracteristics of ZVS-CV Cuk converter.

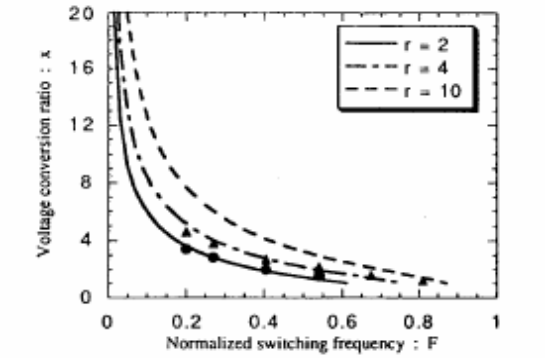
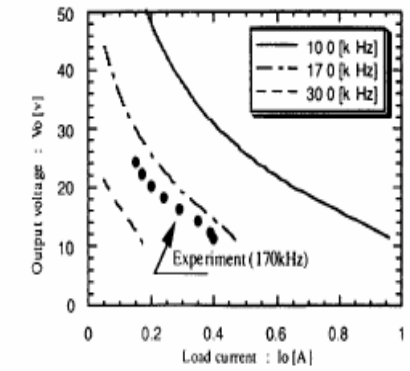


Fig.11 Control chracteristics of ZVS-CV Cuk converter.



V_i = 5 [v] , L_1 = 517 [μH]
L_r = 5.14 [μH] , C_1 = 100 [μF]
C'_1 = 14 [nF] , C'_d = 2.7 [nF]

Fig.12 Load chracteristics of ZVS-CV boost converter.

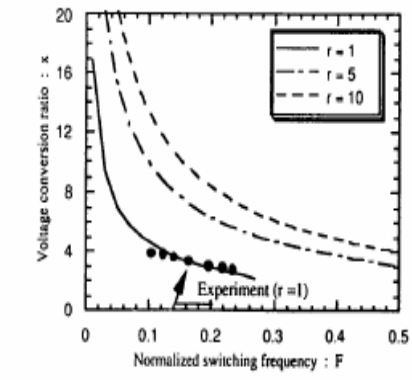


Fig.13 Control chracteristics of ZVS-CV boost converter.

6. CONCLUSIONS

The ZVS-CV converters have been proposed by adding a commutation inductor circuit in parallel with the switch cell in the conventional basic PWM converters. The commutation inductor circuit is a quite simple circuit composed of a series connection of a resonant inductor and a relatively large capacitor. The steady-state analysis has been carried out, as an example. for the ZVS-CV Cuk and boost converters, and its validity has been confirmed by experimental results. In conclusion, the features of the proposed ZVS-CV converters are summarized as follows:

1) A entire family of ZVS-CV converters are constructed with the minimum switches (one transistor and one diode) and a small number of passive elements.
2) Transistor tum-on loss and turn-on noise are sufficiently Reduced
3) Both transistor and diode have the minimum voltage stress.
4) Although the frequency control for the output voltage regulation is needed, it is easy to control only one active switch.
5) The voltage conversion ratio for ZVS-CV operation is limited in the lower side.

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