Design and analysis of ZVZCS converter with active clamping

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Abstract-The design and analysis of ZVZCS converter with active clamping is proposed. By adding a secondary active clamp and controlling the clamp switch moderately, ZVS (for leading leg switches) and ZCS (for lagging leg switches) are achieved without any lossy components, the reverse avalanche break down of leading-leg IGHTs or the saturable reactor in the primary**.** Many advantages including simple circuit topology, high efficiency, and low cost make the new converter attractive for high voltage and high power (> 10 kW) applications. The principle of operation is explained and analyzed. The features and design considerations of the new converter are also illustrated and verified on an 1.8 kW, 100 kHz IGBT based experimental circuit.

1.INTRODUCTION

IGBTs are widely used in the switching power conversion applications because of their distinctive advantages such as easiness in drive and high frequency switching capability. The performance of IGBTs has been continuously improved and the latest IGBTs can be operated at 10-20 kHz without including any snubber circuit. More over, IGBTs are replacing MOSFETs for the several or several tens kilo-watts power range applications since IGBTs can handle higher voltage and power with higher power density and lower cost comparing to MOSFETs. The maximum operating frequency of IGBTs is limited to 20-30 kHz [11 because of their current tailing problem. To operate IGBTs at high switching frequencies, it is required to reduce the turn-off switching loss. ZVS with a substantial external capacitor or ZClS can be a solution. The ZCS, however, is deemed more effective since the minority carrier is swept out before turning off.

ZVS-FB-PWM converters have received considerable attention in recent years. This converter is controlled by phase shifted PWM technique which enables the use of all parasitic elements in the bridge to provide ZVS conditions for the switches. Distinctive advantages including ZVS with no additional components and low device voltage/current stresses make it very attractive for high frequency, high-power applications where MOSFETs are predominantly used as the power

switches. The IGBTs, however, are not suited for the ZVS-FB-PWM converter because the ZVS range is quite limited unless the leakage inductance is very large. In addition, several demerits such as duty cycle loss and parasitic ringing in the secondary limit the maximum power rating of the converter. To apply IGBTs for high frequency converter, a ZVZCS-FB-PWM converter was presented. IGBTs with no anti parallel diodes are used for all primary switches. During freewheeling period, the primary current is reset by using reverse avalanche break down voltage of the leading leg IGBTs, which provides ZCS condition to lagging leg IGBTs. However, it has some drawbacks as follows: The stored energy in the leakage inductance is completely dissipated in the leading-leg IGBTs; The maximum controllable duty cycle is limited since the reverse avalanche breakdown voltage is low (1 5-30V) and fixed. Therefore, the overall efficiency will be deteriorated unless the leakage inductance is very low.

Another approach for ZVZCS-FB-PWM converter was presented**.** By utilizing dc blocking capacitor and adding a saturable inductor in the primary, the primary current during the freewheeling period is reset which provides ZCS condition to the lagging leg switches. Meanwhile, the leading leg switches are still operated with ZVS. The stored energy in the leakage inductance is recovered to the dc blocking capacitor and finally transferred to the load. By increasing the blocking capacitor voltage (i.e. by reducing capacitance), wide duty cycle control range is attainable even when the leakage inductance is relatively large. This converter can be effectively applied to several kW power range applications. Some demerits including loss in saturable inductor and its cooling problem hinder further increase of power level above 10 kW.

This paper proposes a novel ZVZCS-FB-PWM converter to improve the performance of the previously presented ZVZCS-FB-PWM converters. The ZVS mechanism of leading leg switches is the same as that of the converters [2-5,8]. The ZCS of lagging leg switches, however, are achieved by adding an active clamp in the secondary rectifier and controlling it moderately. No lossy components are added to achieve ZVZCS operation and the duty cycle loss is almost negligible. So, the new converter overcomes most of the limitations of the soft switching full bridge PWM converters, which makes the new converter very attractive for high voltage, high power (> 10 kW) applications where IGBTs are predominantly used as the power switches. The basic operation and features of the proposed converter are described. A **1.8** kW, 100 kHz prototype has been built using IGBTs (a MOSFET for the clamp switch) and tested to verify the principle of operation.

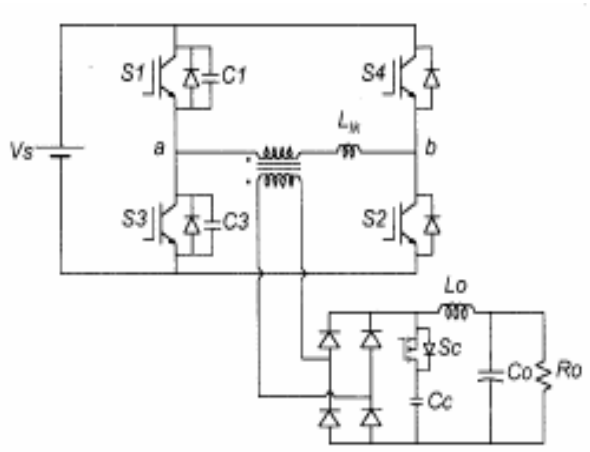

Fig. 1 Circuit topology of the proposed ZVZCS full bridge PWM converter.

2. Operation and Analysis

The basic structure of the proposed ZVZCS-FBPWM converter is the same as that of the ZVS-FB-PWM converter with the active clamp in the secondary side. The control of the primary switches is also the same, phase shift PWM control. The control of active clamp is a little different, which will be explained later in this section.

To illustrate steady state operation, several assumptions are made as follows:

. All components are ideal,

. Output filter inductor is large enough to be treated as a constant current source during a switching period.,

. Clamp capacitor is large enough to be treated as a constant voltage source During a switching period.

The new converter has eight operating modes within each operating half-cycle. The equivalent circuits and operation waveforms are shown in Figs. 2 and 3, respectively.

Mode 1: S1 and S2 are conducting and the input power is delivered to the output. At the beginning of this mode, the rectifier voltage which was increasing is clamped by Vc through the body diode of Sc. The stored energy in the leakage inductance which is generated by the resonance between the leakage inductance and parasitic capacitance is recovered to the clamp capacitor. So, the primary current is decreased as follows:

$$I_P(t) = (1/L_{lk})\{V_s-(V_c/n)\}.t \qquad (1)$$

where ***n*** is transformer turn ratio and the clamp capacitor current can be expressed as follows:

$$I_C = (I_P/n)-I_O \qquad (2)$$

This mode ends when I, becomes zero. The duration of this mode depends on the leakage inductance and the junction capacitance and reverse recovery time of the rectifier diodes.

Mode 2: The body diode of Sc blocks and the secondary rectifier voltage becomes

$$V_{rec} = n V_S \qquad (3)$$

The S1 and S2 are still on and the powering mode is sustained during this mode.

Mode 3: According to the given duty cycle, S1 is turned off and then, the reflected load current to the primary charges C1 and discharges C3. The switch voltage increases linearly as follows:

$$V_{sl}(t) = \{(n I_O)/(C_1+ C_3)\}.t \qquad (4)$$

The turn-off process of S1 is low loss if the external capacitor is large enough to hold the switch voltage at near zero during the switch turn-off time. During this mode, the secondary rectifier voltage is also decreased with almost same rate. At the end of this mode, D3 is turned on.

Mode 4: After D3 starts conducting, S3 can be turned on with ZVS. The load current freewheels through the primary side, D3 and S2. To reset the primary current, the clamp switch is turned on and then, the rectifier voltage becomes Vc. This voltage is applied to the leakage inductance and the primary current is linearly decreased with the slope of $Vc/n\ L_{lk}$ k and I_C is linearly increased. The primary current reaches zero at the end of this mode.

Mode 5: The rectifier diodes are turned off since the primary current is zero and ***Sc*** is still on. During this mode, the primary current sustained at zero and Cc supplies whole load current.

Mode 6: The Sc is turned off and then the rectifier voltage is dropped to zero. The load current freewheels through the rectifier itself. No current flows through the primary.

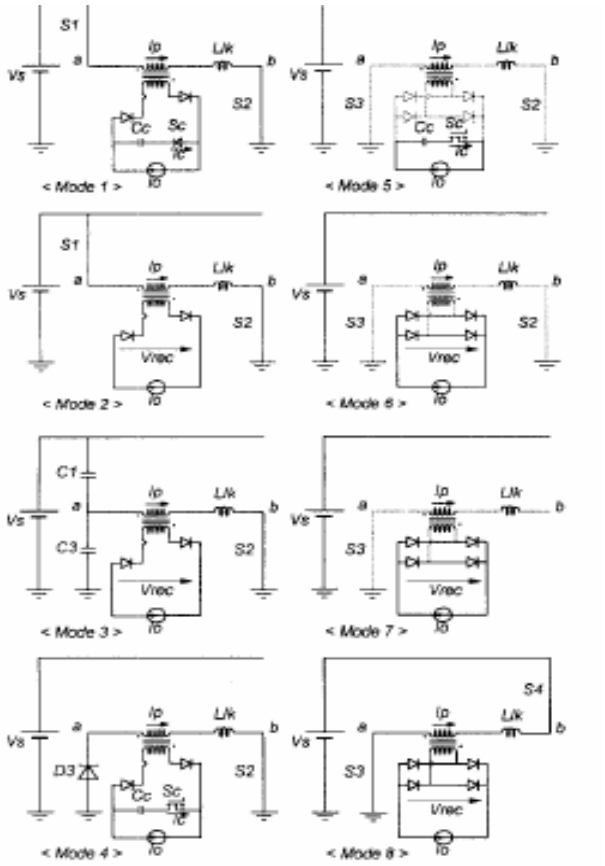

Fig. 2 Operation mode diagrams for eight modes.

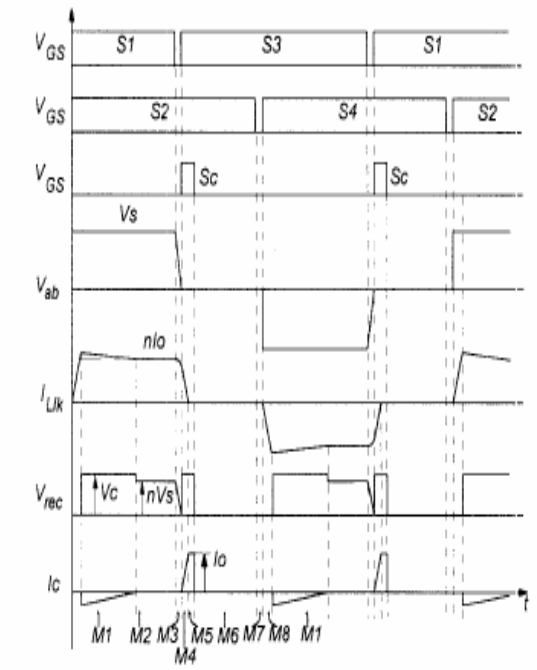

Fig. 3 Operation waveforms.

Mode 7: At the end of freewheeling mode, S2 can be turned off with ZCS. No tail current exists since all minority carriers are eliminated by recombination. This mode is dead time between S2 and S4.

Mode 8: To terminate from freewheeling mode, S4 is turned on. This turn-on process is also ZCS since the primary current can not be changed abruptly and no diode reverse recovery is involved. The primary current Ip is linearly increased with the slop of Vs/ $L_{l\,k}$ .The rectifier voltage is still zero. This is the end of an operating half-cycle.

3. Features of the Proposed Converter

3. 1. *Eflective Soft Switching (ZVZCS)*

Soft switching mechanism (ZVS for leading-leg switches and ZCS for lagging leg switches) of the proposed converter has exactly the same as those of the ZVZCS converters. The converters use lossy components to achieve ZCS of

lagging leg switches. The stored energy in the leakage inductance is completely dissipated in the leading-leg IGBTs during freewheeling mode or there exists the core loss of saturable reactor. In addition, additional losses exists in the clamp resistor for both converters if the passive clamp circuit is used to clamp the secondary rectifier voltage. Therefore, both converters have limited power range (several kW). In the proposed converter, however, ZCS of lagging-leg switches is achieved more efficiently by modifying control of the active clamp. No lossy components are involved in achieving ZCS and no parasitic ringing is generated in the secondary rectifier. So, the proposed converter can handle higher power level (> 10 kW).

The ZCS of lagging-leg switches is achieved with whole load ranges and the ZVS of the leading-leg switches is also achieved with wide load range.

3. 2..*More Reduced Conduction Loss*

The primary voltage, current, and the secondary voltage of the proposed converter are compared to those of the ZVS , and the ZVZCS converters as shown in Fig. 4. The ZVS converter has considerable duty cycle loss since large leakage inductance is required to obtain wide ZVS range. The ZVZCS converters improves the overall efficiency by removing the freewheeling current in the primary and reducing the duty cycle loss. The maximum duty cycle, however, is limited by the primary current reset-time, Treset which is determined by the applied voltage to the leakage inductance $V_{L\,l\,k}$ during freewheeling period as follows:

$$T_{RESET} = L_{l\,k}\{(n\,I_O)/\,V_{L\,l\,k}\} \qquad (5)$$

The Treset of the converters is considerably large since low voltage (several tens volts) is applied to the leakage inductance, which affects the overall efficiency as same as the duty cycle loss. In the proposed ZVZCS converter, however, a small Treset achieved since the high voltage (V_C/n) is applied to the leakage inductance. So, the overall efficiency of the proposed converter is improved due to low duty cycle loss as well as small Treset.

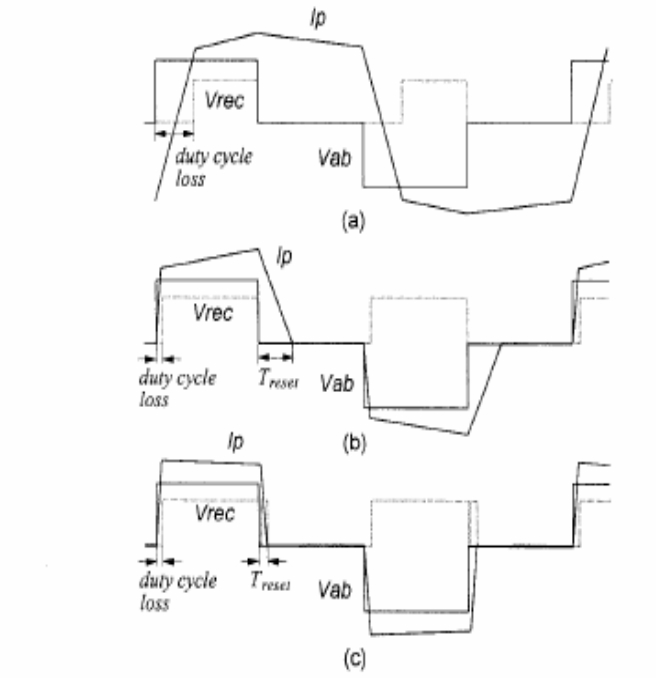

Fig. 4 Comparison of the simplified waveforms of primary voltages and currents and secondary rectifier voltages: (a) ZVS PWM converter, (b) ZVZCS PWM converters [7,8], (c) proposed converter.

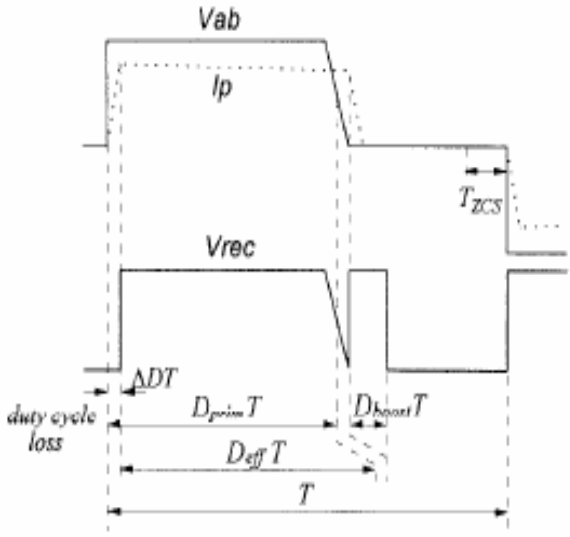

Fig. 5 Primary and secondary rectifier voltage waveforms.

3. 3.*Duty Cycle Boost Effect*

The secondary rectifier duty cycle is usually lower than that of the primary because of the duty cycle loss. In the proposed converter, however, the rectifier duty cycle can be
higher than that of the primary as shown in Fig. 5. This phenomenon is named as *duty **cycle** boost **effect.*** The duty cycle boost effect is caused by the operation of the active clamp from the beginning of freewheeling period to provide ZCS condition to the lagging-leg switches. This means that the stored energy in the leakage inductance is recovered to the clamp capacitor and finally transferred to the load by means of the duty cycle boost effect. This feature is very important for the ZVZCS converters which use IGBTs for main switches. The primary duty cycle can not be increased to near unity since the minimum dead-time is required to achieve a complete ZCS turn-off of the lagging-leg switches which is the time for minority carrier recombination of IGBTs. The effective duty cycle of the proposed converter, however, can be increased to near unity due to the duty cycle boost effect. The effective duty cycle of the proposed converter can be expressed as follows:

$$D_{eff} = D_{prim} - \Delta D + D_{boost} \quad (6)$$

where ΔD is the duty cycle loss. The D_{boost} is determined directly by the turn-on time of the clamp switch. The duty cycle boost effect also helps to improve the overall efficiency.

4. Design Considerations

4.1. *Decision of Dead Times*

An appropriate dead time is required for both leading and lagging-leg switches to achieve maximum performance. Dead time for leading-leg switches: The dead time for leading-leg switches is determined by two factors, the ZVS range and the maximum duty cycle of the primary side. The minimum dead time is determined by ZVS range as follows:

$$T_{d,\,lead} \geq (C1+C3)\{Vs/\, I_{O,ZVS}\} \quad (7)$$

where $I_{O,ZVS}$ is given ZVS range as one of design parameters. The maximum dead time is limited by the maximum duty cycle of the primary side.

Dead time for lagging-leg switches: The minimum dead time of lagging-leg switches is determined by the time T_{ZCS} to achieve a complete ZCS of the lagging-leg switches as
follows:

$$T_{d,\,lag} \geq T_{ZCS} \quad (8)$$

where the T_{ZCS} is the minority carrier recombination time of waveforms**.** IGBTs. The maximum dead time is also limited by the maximum duty cycle of the primary side.

4.2. *Decision of Dead Times*

The illustrative waveforms of the secondary rectifier voltage and the clamp capacitor current according to the turn-on time of Sc are depicted in Fig. ***6.*** To achieve a complete ZCS of lagging-leg switches, the primary current should be reset. The required turn-on time Tsc of Sc is obtained as follows:

$$Tsc \geq \{(n2\ L_{l\,k})/V_c\}\ I_{o,\,max} \quad (9)$$

The clamp capacitor current is abruptly increased according to the on-time Tsc as shown in Fig. ***6.*** Therefore, the Tsc need to be kept as small as possible to reduce the conduction
loss of clamp switch and in turn allow use of a small switch for Sc. The clamp capacitor voltage is regulated automatically as shown in Fig. **6.**

4.3. ***Active Clamp Circuit for Center-Tapped Transformer***

The proposed ZVZCS power conversion technique can also be applied for the center-tapped transformer as shown in Fig. **7.** The basic operation principle is exactly the
same as that of the simple output transformer except diode voltage.

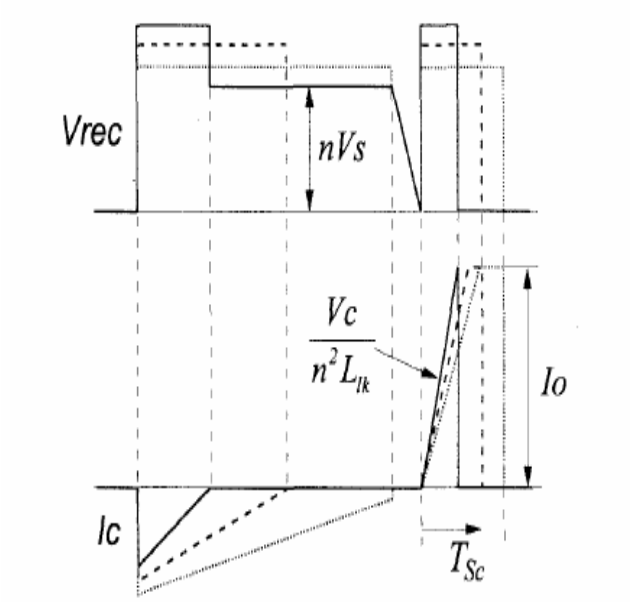

Fig. 6 Illustrative waveforms of the rectifier voltage and the clamp capacitor current.

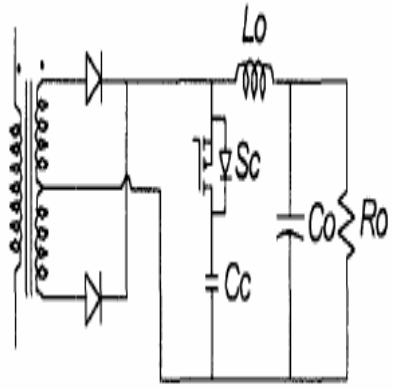

Fig. 7 Circuit diagram of the active clamp circuit for a center tapped transformer.

5. Experimental Results

An 1.8 kW, 100 kHz prototype of the proposed ZVZCS-FB-PWM converter has been built and tested to verify the principle of operation. Fig. **8** shows the experimental circuit with the part numbers and the circuit parameters. The transformer is built using an EE/55/55 core with the turns ratio of ***Np:Ns=28:5.*** The leakage inductance measured at the switching frequency is 3.6 uH. IRGPC40UD2 IGBTs are used for the primary switches. The recommended switching frequency for the IRGPC40UD2 provided by the data sheet is only 10-20 kHz. **As** will be shown, these IGBTs can be operated at 100 kHz without any detrimental effects on the efficiency.

Fig. 9 shows the waveforms of the primary voltage and current and the secondary rectifier voltage at full load (nominal duty cycle of 0.78**)** and Fig. 10 shows the extended
waveforms at the switching transitions of leading and lagging legs. All waveforms are well matched with the expected ones. The primary voltage shows slow down slope due to the external capacitors added to the leading-leg switches and fast up slope. The duty cycle loss is about 0.lus. The primary current is quickly reset right after the primary voltage is dropped to zero and sustained during the freewheeling period. The primary current reset time is only 0.15 us. The turn-on time of the active switch is about 0.35 us. Fig. 11 shows the extended switching waveforms of leading-leg switches. It can be seen that the anti-parallel diode current flows for short time and stays zero and thus, a complete ZVS turn-on is achieved. The tail current is seen but the turn-off switching loss is remarkably

reduced comparing to hard switching since the rising slope of the switch voltage is slow. The ZVS range for the leading-leg switches is about 20 % of full load. Fig. 12 shows the extended switching waveforms of lagging-leg switches. It can be seen that a complete ZCS turn-off is achieved since the primary current is zero during the whole freewheeling period and the turn-on process of the other switch is almost ZCS. Small pulse current during turn-on transition is the charging current of the switch output
capacitor. Fig. 13 shows the waveforms of the secondary active clamp. The clamp switch is turned-on for very short time comparing 1.0 the operating period (7 %). The rectifier voltage waveform shows a little noisy since the clamp switch operates under hard switching. The clamp capacitor current waveform is the same as the expected. The maximum measured efficiency is about 94 %.

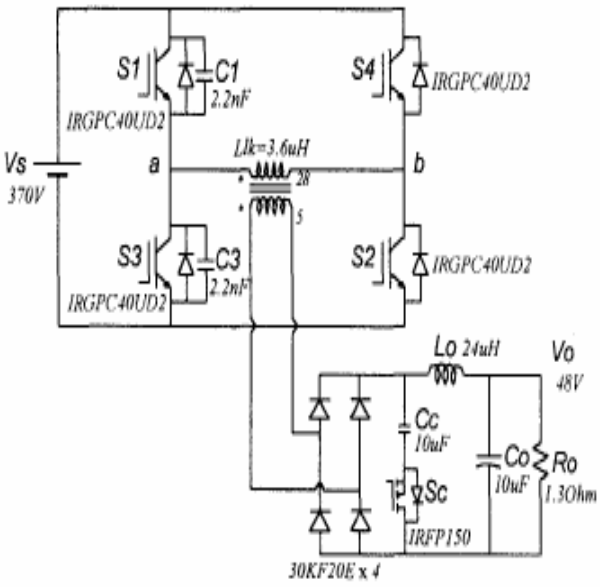

Fig. 8 Experimental circuit diagram of the proposed converter.

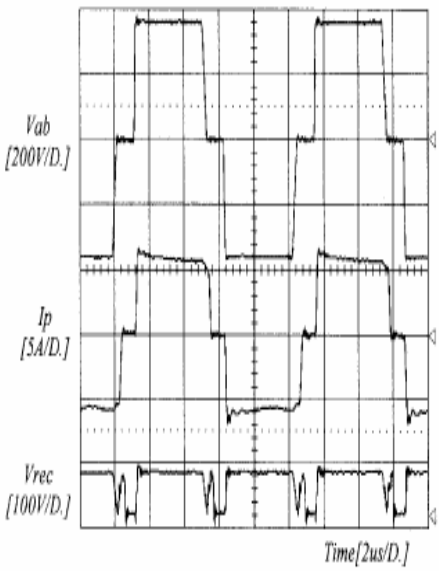

Fig. 9 Experimental waveforms of primary voltage and current and secondary rectifier voltage.

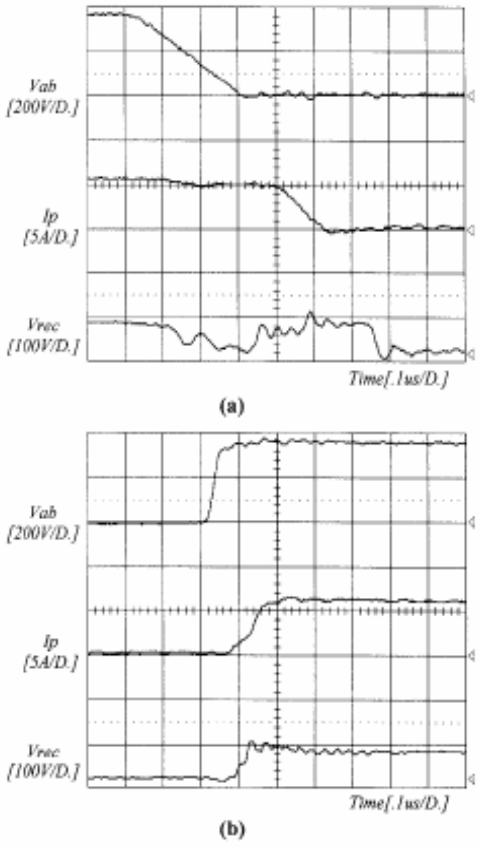

Fig. 10 Extended waveforms at switching transitions: (a) leading-leg, (b) lagging-leg.

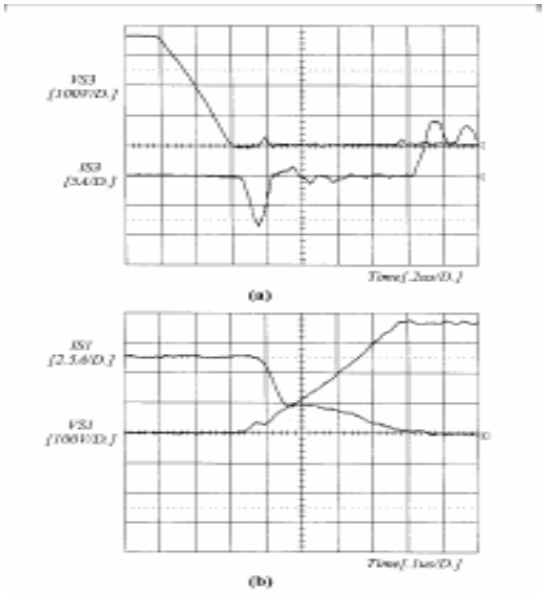

Fig. 11 Extended ZVS switching waveforms of leading leg switches: (a) turn-on, (b) turn-off.

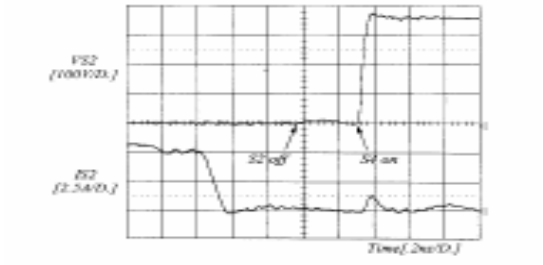

Fig. 12 Extended ZCS waveforms of lagging-leg switches.

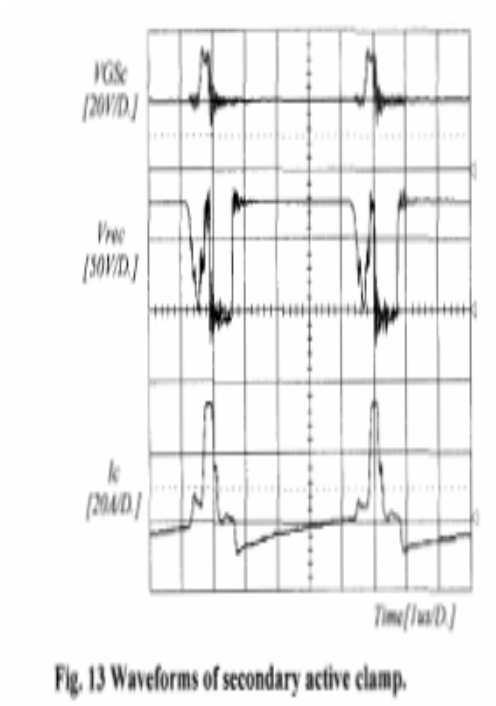

Fig. 13 Waveforms of secondary active clamp.

6. CONCLUSIONS

A novel ZVZCS-FB-PWh4 converter using secondary active clamp is presented. The operation, features and design considerations are illustrated and verified by the experimental results on a 1.8 kW, 100 kHz IGBT based.

It is shown that ZVS for leading leg switches and ZCS for lagging leg switches are achieved by the help of the active clamp. The efficiency attained at full load was about 94 **%.** The proposed converter has distinctive advantages over the previously presented ZVZCS converters as follows:

a) ZVS and ZCS without any lossy components;
b) wide ZVS and ZCS range;
c) high duty cycle is attainable;
d) more reduced conduction loss in the primary;
e) no severe parasitic ringing.

Many advantages of the new circuit makes the proposed converter very promising for high voltage (400-800 V), high power (> 10 kW) applications with high power density.

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