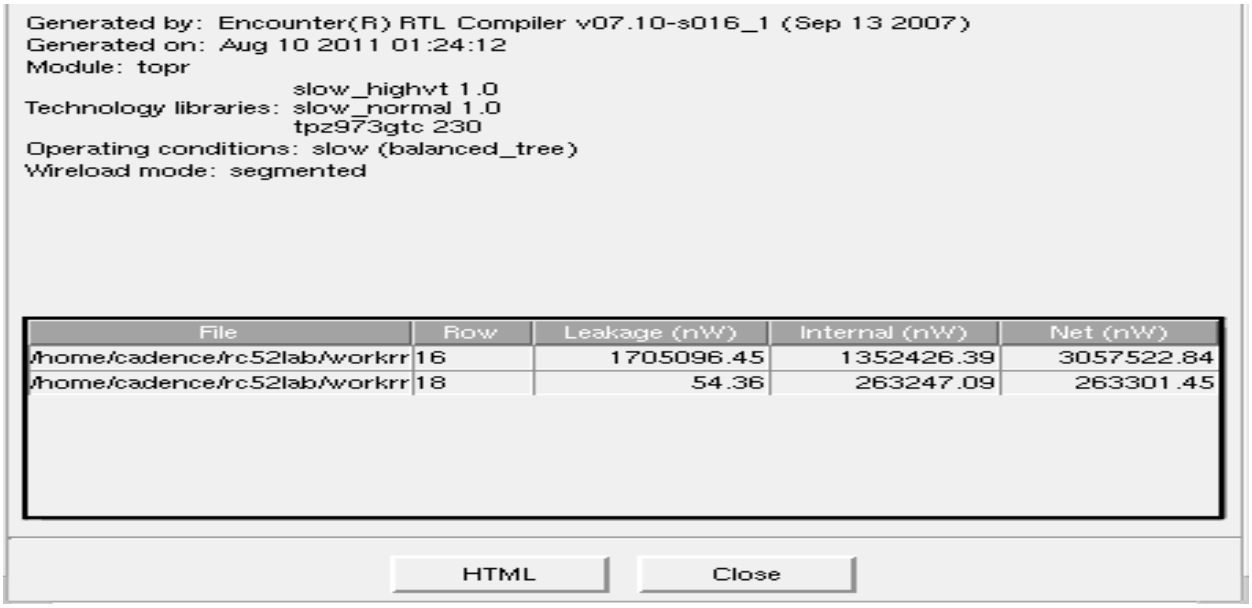

Figure 12: Report RTL Power

7. Tools

IUS – Intensive Unified Simulator
IUS is used to determine
1. Logic of the design through waveforms
2. Timing analysis
3. Instantaneous power

Encounter RTL Compiler

1. This software is 52 version. By using RTL compiler we can generate the NETLIST which describes the number of gates, delays, power consumption, etc.

2. By using RTL Compiler, we have designed input/output padding for the RISC Processor which will protect from power supply hazards.

SOC is used to determine post layout area of the chip, clock tree synthesis, power considerations, ordering of the pins, floor planning, etc.The design is implemented by using all the software which has TSMC (Taiwan Semi Conductor Manufacturing Corporation) technology libraries.

8. Conclusion

The 64 bit RISC Processor with an instruction set has been designed. Each instruction is designed in one clock cycle. The design is verified through exhaustive simulation and all the constraints like clock, power, delays, etc. have been implemented using RTL Compiler and SOC Encounter.

9. References

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