











Figure 5: Simulink model of DLX based ALU

**VI. Results**

A DLX based ALU is designed using HDL and a reusable Simulink model is developed using HDL modules. The implementation of this model is done on to FPGA device using System Generator®. The device utilization summary after synthesization for xc4vsx35-12ff668 of Virtex 4 series is given in the table 4-

Table 4: Device utilization summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	462	15360	3%
Number of Slice Flip Flops	114	30720	0%
Number of 4 input LUTs	808	30720	2%
Number of bonded IOBs	170	448	37%
Number of GCLKs	3	32	9%

**Conclusion**

HDL provides us the capability of hardware designing and by using Simulink Modeling Methodology, reusable models of these devices can be easily developed for the hardware implementation. As well as there is no need to design every module in the HDL, some basic available modules can be used from the Simulink library itself.

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