

An Effective Leading Zero Anticipation for High Speed Floating Point Addition and Subtraction

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Abstract

A new leading-zero anticipatory (LZA) logic for high-speed floating-point addition and subtraction is proposed. The pre-decoding for normalization concurrently with addition for the significant is carried out in this logic. Shift operation of normalization in parallel with the rounding operation is also performed. The use of simple Boolean algebra allows the proposed logic to be constructed from a simple CMOS circuit.

2. Introduction

The floating point units play an important part in the modern microprocessors. To get an efficient design the delay and energy consumption should be optimized. The normalization is the main operation of floating point data path, the output of the floating point operation should be normalized according to the IEEE 754 format [1]. The normalization involves leading zero counter and a normalization shifter. In all the cases a leading zero anticipator (LZA) is employed to increase the computation speed[2]. Several floating-point chips currently in production have adopted the LZA approach to reduce their delay time. The LZA logic is used to predict the pseudo result, the clear and thorough overview of the efficient solution can be found.

This paper proposes a new leading zero anticipation method. This method is based on Boolean algebra structure and can be realised using fast logic circuits. The rest of this paper is organized as follows the section 2 describes the existing leading zero anticipation method, the section 3 describes the proposed leading zero anticipation method and comparison with the existing leading zero anticipating logic, section 4 gives the results of proposed leading zero anticipation logic, section 5 concludes the paper and followed by references.

2. Existing Leading Zero Anticipation Method

This section discusses about the existing leading zero anticipation method. In the existing method the

detection is restricted to only leading zeros or leading ones [3]. When the circuit for detection of leading zeros does not need to consider cases where leading ones might result [4], then the leading zero indicator can be simplified to the equation below

$$F = \bar{T}_i \bar{Z}_{i+1}, i \geq 0$$

Here a comparison of the operands is performed to ensure that only the smaller operand is complemented during subtraction. Other designs where this could be applied would be where separate adders are provided for use when the exponents are equal. One adder calculates A-B and the other calculates B-A, and the result from the adder producing a carry out is selected. Each adder then needs only a leading zero detector [5]. The detection of the number of leading zeros to start in parallel with swapping, aligning and inverting the operands. When the exponents differ by one, the presumed smaller operand is shifted right one place and then inverted [6]. Since the operands must be normalized, the function in the first bit must be G, and therefore the number of leading zeros is determined by the number of following bit positions that are Zs [3]-[5]. Therefore, the leading zero indicator in each following bit position is $F = \bar{Z}_{i+1}$.

3. Proposed Leading Zero Anticipation Method

This section discusses about the proposed leading zero anticipation method. The proposed method is based on the restricted case that is A is always greater than or equal to B. According to this case A-B is always positive and A+B is also positive that is the result is always positive. Proposed Anticipation logic is based on generation of intermediate Difference and Borrow strings.

The proposed leading zero anticipation in addition can be explained by considering the addition example, consider A= 0010 0110 and B= 0000 1010, now the predicted string F_{add} is obtained as shown below.

$$\begin{array}{r}
 A_{in} \rightarrow 0010\ 0110 \\
 B_{in} \rightarrow 0000\ 1010 \\
 \hline
 F_{add} \rightarrow 0011\ 0000
 \end{array}$$

By the above example we can find that number of leading zeros in F_{add} is equal to number of leading zeros in A, that is the number of leading zeros in result are always equal to or one less than operand A.

The subtraction in the proposed leading zero anticipation is explained considering the subtraction example, consider A= 0011 0110 and B= 0001 1010, now the propagate(P), borrow(B), difference(D) and the predicted string F_{sub} is obtained as shown below

$$\begin{array}{r}
 A_{in} = 0011\ 0110 \\
 B_{in} = 0001\ 1010 \\
 \hline
 P = 0010\ 1100 \\
 B = 0000\ 1000 \\
 \hline
 D = 0001\ 1100 \\
 \hline
 F_{sub} = 0011\ 1100
 \end{array}$$

From the above example, the F_{sub} is proposed as $F_{sub}(0)$ is equal to $P(0)$ and $F_{sub}[n] = P[n] \wedge B[n-1]$ where $B[n] = \bar{A}[n] \cdot B[n]$. The addition and subtraction are proposed by the Boolean algebra expressions as shown above. The proposed leading zero anticipation method is accurate and fast when compared with the existing leading zero anticipation method and overrides it in all aspects. To contain both the addition and subtraction a multiplexer is used to select the respective operation. The figure1 shows the proposed LZA.

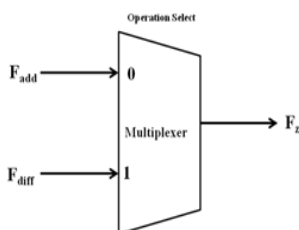


Fig1:-Proposed LZA

The proposed LZA is more accurate than the existing LZA method this can be observed in following four cases. Any combination of input patterns falls into one of these patterns in the cases considered. In case 1 the number of leading zeros in the final result are 7 which is equal to the proposed LZA where the Existing LZA has 11 leading zeros in its result, in case 2 the number of leading zeros in the final result are 0 which is equal to the proposed LZA where the Existing LZA has 2 leading zeros in its result, in case 3 the number of leading zeros in the final result are 11, the proposed LZA has 10 leading zeros where the Existing LZA has 2 leading zeros in its result, in case 4 the number of

leading zeros in the final result are 15 which is equal to the proposed LZA where the Existing LZA has 2 leading zeros in its result.

Case1:-

$$\begin{array}{r}
 A_{in} = 1000\ 0000\ 1010\ 0001 \\
 B_{in} = 0111\ 1111\ 0110\ 1001 \\
 \hline
 P = 1111\ 1111\ 1100\ 1000 \\
 B = 0111\ 1111\ 0100\ 1000 \\
 K = 0000\ 0000\ 0001\ 0110 \\
 \hline
 A-B = 0000\ 0001\ 0011\ 1000
 \end{array}$$

Proposed LZA = 0000 0001 0101 1000

Existing LZA = 0000 0000 0001 001x

Case 2:-

$$\begin{array}{r}
 A_{in} = 1001\ 1100\ 0010\ 0001 \\
 B_{in} = 0001\ 1011\ 1100\ 1001 \\
 \hline
 P = 1000\ 0111\ 1110\ 1000 \\
 B = 0000\ 0011\ 1100\ 1000 \\
 K = 0110\ 0000\ 0001\ 0110
 \end{array}$$

A+B = 1011 0111 1110 1010

Proposed LZA = 1001 1100 0010 0001

Existing LZA = 0011 1000 0001 001x

Case 3:-

$$\begin{array}{r}
 A_{in} = 1001\ 1100\ 1010\ 0001 \\
 B_{in} = 1001\ 1100\ 1000\ 1001 \\
 \hline
 P = 0000\ 0000\ 0010\ 1000 \\
 B = 0000\ 0000\ 0000\ 1000 \\
 K = 0110\ 0011\ 0101\ 0110
 \end{array}$$

A-B = 0000 0000 0001 1000

Proposed LZA = 0000 0000 0011 1000

Existing LZA = 0011 1001 0101 001x

Case 4:-

$$\begin{array}{r}
 A_{in} = 1001\ 1100\ 1010\ 1000 \\
 B_{in} = 1001\ 1100\ 1010\ 0111 \\
 \hline
 P = 0000\ 0000\ 0000\ 1111 \\
 B = 0000\ 0000\ 0000\ 0111 \\
 K = 0110\ 0011\ 0101\ 0000
 \end{array}$$

A-B = 0000 0000 0000 0001

Proposed LZA = 0000 0000 0000 0001

Existing LZA = 0011 1001 0101 000x

The above cases show that the proposed LZA is more accurate than the existing LZA method.

4. Results

The proposed Leading Zero Anticipation method is implemented on Spartan 3E family device XC3S500E package FG320 with speed grade -5.

The delay characteristics and the occupancy rates are compared with the existing method and tabulated below. From the results below the number of slices occupied by the proposed method are 32 which is less than 1% occupancy rate. The delay is the total combinational delay and is obtained as 6.347ns. The number of 4 input LUTs are 32 out of 9312 and the number of bonded IOBs are 97 out of 232. The proposed Leading Zero anticipation is implemented using Verilog HDL on Xilinx ISE 10.1 tool.

Table 1:- Synthesis Result of Proposed LZA

Logic Utilization	Proposed LZA	Available
Number of Slices	32	4656
Number of 4 Input LUTs	32	9312
Number of bonded IOBs	97	232
Combinational Path Delay	6.347 ns	-

The simulation result of the proposed LZA is shown in the figure 2 below

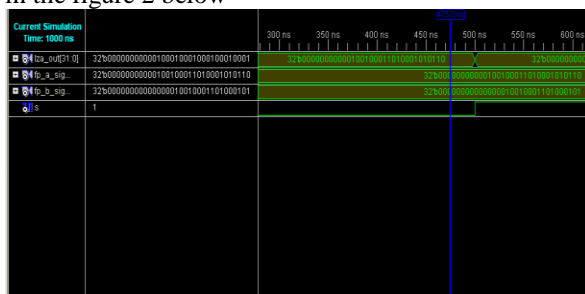


Fig2:- Simulation Result of Proposed LZA

5. Conclusion

In this paper a Leading Zero Anticipation Method is proposed and the accuracy of the proposed LZA is significantly increased when compared with the existing method. Examples are considered and proved that the proposed method is more accurate than the existing LZA method. The design is implemented using Verilog HDL and verified using extensive directed-random vectors. The proposed leading zero anticipation method can be utilised in many application areas like RISC, CISC, Microprocessors and DSP. This proposed LZA can be effectively utilised in high speed floating point units.

References

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