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Crosstalk and Crosstalk Delay Minimization in On-Chip DSM VLSI Interconnects

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Abstract

In On-chip DSM and UDSM VLSI Circuits because of increase device densitities and operating clock frequency the crosstalk noise, crosstalk induced delay, interconnect delay , signal integrity affect the performance and reliability of the chip. Due to increase in operating frequency beyond GHz range inductive effects are dominant over capacitive effect. Therefore, the coding methods used in RC Modeled are not suitable in high frequency application circuits. This research work includes TSPICE simulation of encoder based on modified boundary shift coding used to reduce inductance dominant crosstalk in coupled RLC modeled interconnects.

Keywords- Crosstalk, Crosstalk Delay, Interconnect delay, Boundary shift Code, Inductive effects

I. INTRODUCTION

As VLSI technology has marched into the DSM/UDSM regime, bus based interconnect has become bottleneck in On-chip systems. In SoC designs where wide and long buses are used interconnect delays dominate over device delay. The crosstalk in on-chip buses is highly dependent on the data patterns transmitted on the bus [10].

On-chip interconnect delay also suffers from various kind of DSM noise sources like power-grid fluctuations, electromagnetic noise, and alpha particle radiation. Defects in manufacturing also cause an unavoidable error in the systems. These induced errors generates serious data transmission reliability concerns for interconnects. Therefore, error-correction scheme is required for on-chip interconnects [2, 11].

In on-chip due to low operating clock frequency mainly source of noise is parasitic capacitance and interconnect can be modeled as RC netlist for timing and noise prediction in design and automation tools [3]. With the increase in operating clock frequency and ever growing length of interconnect the interconnect effects are not limited to RC models [1].

The propagation delay in inductive dominant buses mainly depends upon the transition patterns transmitted on the bus. The noise generated due theses switching patterns is because of changes in current through various parasitic inductances. The grounds bounce noise (i.e. noise induced in supply and ground voltages in the presence of large currents) is generated because of simultaneously switching of input output drivers and due to internal circuits [4, 11].

The inductive effects generated in on-chip interconnects causes signal integrity, reliability, and drop in performance [5].The worst-case switching patterns for an RLC modeled interconnect lines have been investigated in [7] [8]. In RLC modeled interconnects when all the neighboring wires simultaneously switch in the same direction similar to the victim wires, a current of different direction to that of victim wire currents generates and results in delay and noise on the victim line, that is higher when the signals switch in the same direction [11].

Worst-case switching pattern for 3-bit bus in an inductive-coupling dominant interconnects are Type-0 and Type-1 and the worst-case switching pattern in a capacitive- dominant interconnect are Type-4 & Type-5 on the contrary, worst case switching pattern of a coupling *RLC* line is the best-case pattern of a coupling *RC* line [1,11].

This paper mainly deals in TSPICE simulation of proposed encoder based on modified boundary shift encoding method [6, 11], which is used to reduce inductive-coupling effects in terms of reduction in propagation delay, crosstalk, and chip size of encoder, and decoder of RLC modeled interconnects.

II. CROSSTALK IN RLC MODELED INTERCONNECTS

The coupling between the groups of the three wires is classified into five Types depending upon the nature of transitions of signals in the wire that are Type-0, Type-1, Type-2, Type-3, Type-4, and Type 5 shown in table-1[1].

The inductive effects are maximum when all the buses switch in the same direction simultaneously. Therefore, the inductive effects are maximum in case of Type 1 type of coupling. When two wires switch in same direction simultaneously in Type 2 & Type 3 crosstalk class then inductive coupling exist upto some extent while capacitive effects are minimum and in Type 4 and Type 5 type of crosstalk classes capacitive effects are maximum and inductive effects are minimum [1]. The author in this research work proposed an alternative method that can minimize

Type 1 and Type 2 type of inductive effects because beyond GHz frequency range and due to increase in interconnect length inductive effects dominate over capcitive effects that means in such environment croostalk is mainly due to inductive effects. Therefore, to reduce inductive coupling author compares the result of the circuits implemented by using bus invert method and by using boundary shift code.

Table 1. 3-bit bus crosstalk classes and corresponding delays [1].

Crosstalk Class	Transition Patterns (d_{k-1}, d_k, d_{k+1})	Crosstalk
Type 0	↑−↑, ↓−↓, ↑−↓, ↓−↑, ↑−−, −−↓, −−−, −−↑, ↓−−	**0**
Type 1	---, ↑↑↑, ↓↓↓	**1**
Type 2	--↑, ↑--, --↓, ↓--, ↑↑−, ↓↓−, −↑↑, −↓↓	1+γ
Type 3	−↑−, ↑-↑, ↑-↓, −↓−, ↓-↓, ↓-↑, ↓↓↑, ↑↑↓, ↓↑↑, ↑↓↓	1+2γ
Type 4	−↓↑, −↑↓, ↑↓−, ↓↑−	1+3γ
Type 5	↓↑↓, ↑↓↑	1+4γ

*The symbols ↑, ↓, − are used to indicate 0→1, 1→0 and 1→1 (or) 0→0 transitions

III. ENCODER & DECODER DESIGN

The impleenation of encoder and decoder is done by using boundary shift code. Therefore, a dependent boundary in a word as a place where two adjacent bits are the same and it will be denoted by the leftmost bit of the boundary. Two words sharing no dependent boundaries e.g. two words 01100111 and 11001110 have dependent boundaries {1,3,5} and {2,4,7}, respectively. Since there is no overlap transition must be valid.

If it has an overlap in dependent boundaries, transition will create delay in an RLC interconnect. In boundary shift coding, 1-bit circular right shift of a codeword with even boundaries yields a new codeword with no even dependent boundaries. This property is used in generation of error-correcting codes with no odd dependent boundaries. If C be an [n, k, d] code then by duplicating each bit position [2n, k, 2d] C_1 code is obtained with no odd boundaries.since every bit in an odd bit position is followed by a copy that means by alternating between C_1 and shifted version of it, 2n, k, 2d] self shielding C_1 code is obtained. If C_1 code is punctured in the last bit position that means by removing the last bit in every code results in [2n-1, k, 2d-1] code. Now, a shifted version of C_1 will have no common dependent boundaries with C. Therefore, in order to avoid simultaneous switching between two consecutive codewords we will alternate between C and C_1. Usually, codewords is right shifted during odd clock cycle and is kept as it is during even clock cycle. In order to add ECC feature to the CAC code, a single even- parity-check code is used in the codeword instead of a Hamming code. For a *k* bit data buses, a single parity would generate a [*k*+1, *k*, 2] codeword and then, duplicating and shifting will generate a [2*k*+1, *k*, 3] single-error-correcting code [6, 11].

Design of Encoder and decoder is based on boundary shift coding is shown in figure 1 and figure 2. A 4-bit data $\{I_0, I_1, I_2, I_3\}$ when encoded using boundary shift coding method is duplicates all the bits, shift , and adds parity bits to the data bits then 9-bit codeword $\{O_0, O_1, O_2, O_3, O_4, O_5, O_6, O_7, O_8\}$ is generated. This 9-bit code is transmitted and at the receiver end decoder is used to decode 9-bit code into 4-bit data just opposite to encoder. Whenever during transmission error is occurred then one error can be corrected and two errors can be detected because distance in between two codewords is three. 9-wires are required for encoding of 4-bit data buses. Therefore, for n-bit data bus 2n+1 number of wires will be required [11].

IV. SIMULATION RESULTS & DISCUSSION

This method has been simulated in CMOS 180, and 130nm technology by using T-SPICE and found reduction in crosstalk delay and also reduction in crosstalk noise shown in figure 3 & Figure 4 in comparison with Fan et. al. Simulated results shows that when both the circuits are simulated in same environment then proposed technique gives results without crosstalk noise. This is also demonstrated in table 2. This method also reduces chip area by reducing number of transistors in comparison with Fan et al. The number of transistors in proposed method is only 397 while in Fan et al 499. This method requires 37.27% lesser chip area as compared with Fan et al.

Table 1 Comparison of proposed method with Fan et al. in different technology nodes

Technology (nm)	Propagation delay(ns)	Encoding Method	% saving
180	98.283	Fan et al	65.37%
	34.028	Proposed	
130	98.915	Fan et al	65.24%
	34.384	Proposed	

V. CONCLUSION

The inductive coupling in on-chip RLC modeled interconnects in DSM technology is dominant over capacitive coupling when operating clock frequency is beyond GHz range and due to increase in interconnect length. The simulated results shows that the encoder and decoder design

based on proposed boundary shift code is efficient in terms of propagation delay, signal integrity, and lesser die size. The proposed method almost removes the worst-case inductive crosstalk using boundary shift encoding method. This method is also reduces the chip area, propagation delay and the circuit is very simple to implement. The proposed method also corrects single error and detects double errors.

VI. ACKNOWLEDGMENT

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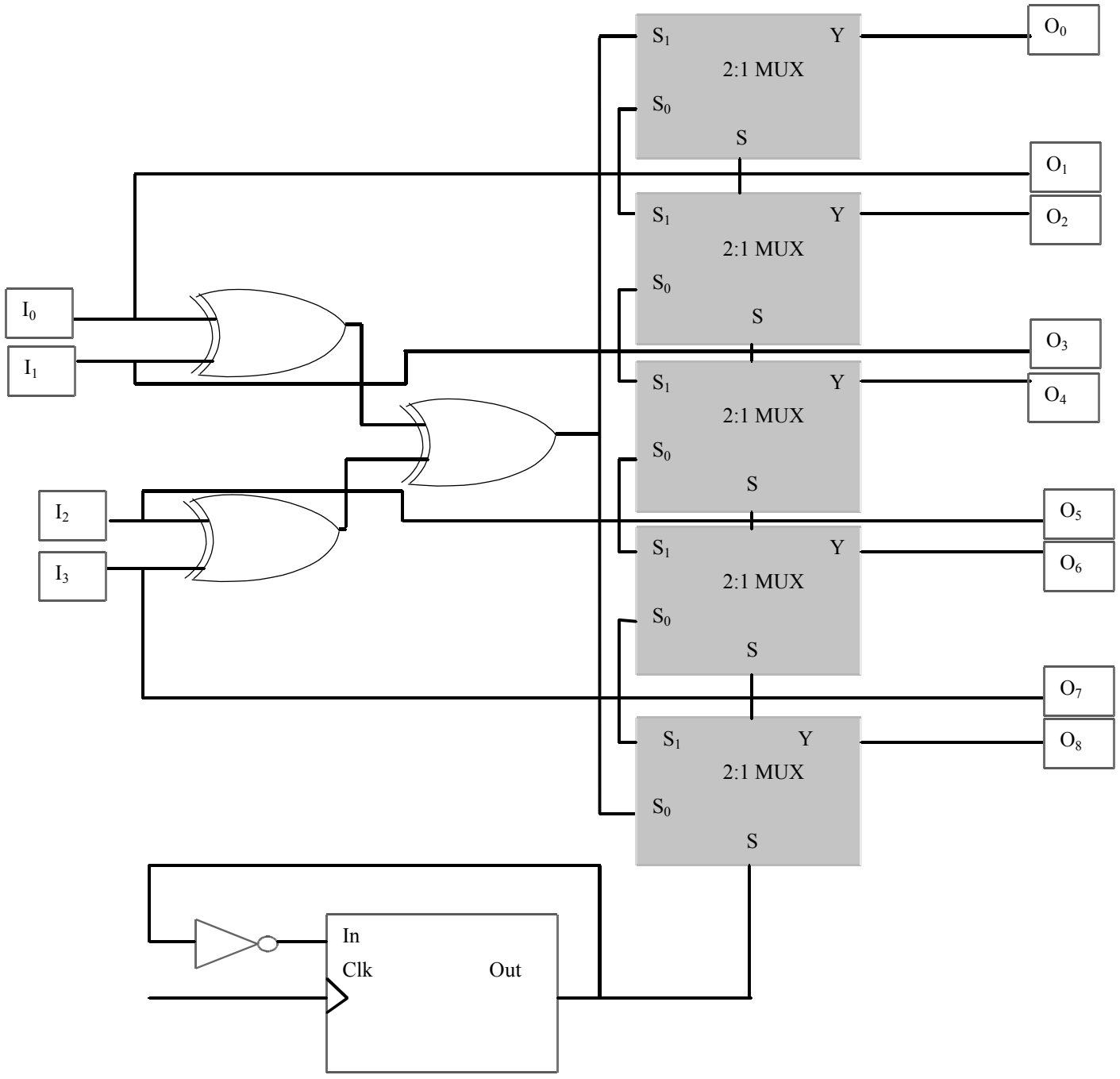

Figure 1. Encoder Circuit based on boundary shift Coding Method [6, 11].

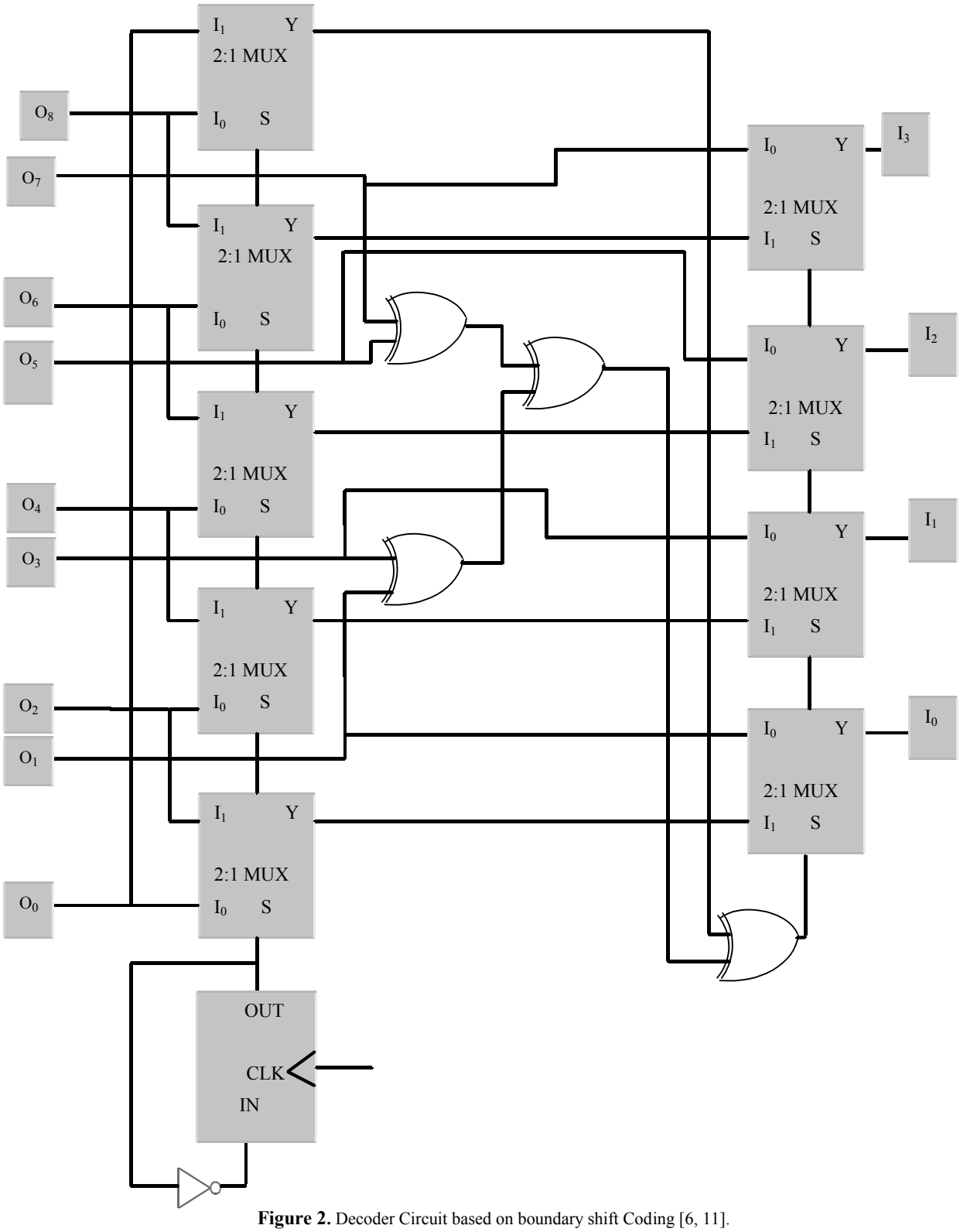

Figure 2. Decoder Circuit based on boundary shift Coding [6, 11].

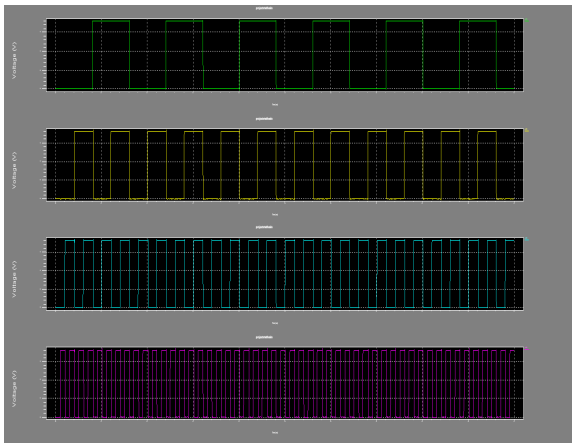

Figure 3(a). Simulation waveform of proposed encoder at 180nm technology node

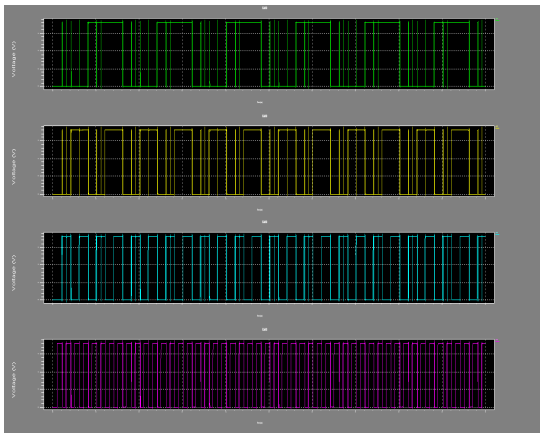

Figure 3(b). Simulation waveform of Fan et al 1 encoder at 180nm technology node

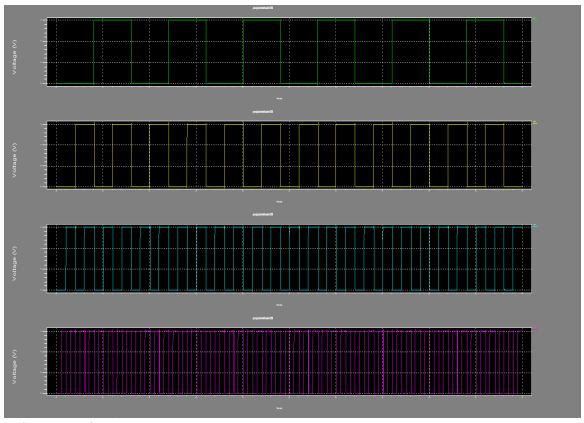

Figure 4(a). Simulation waveform of proposed encoder at 130nm technology node

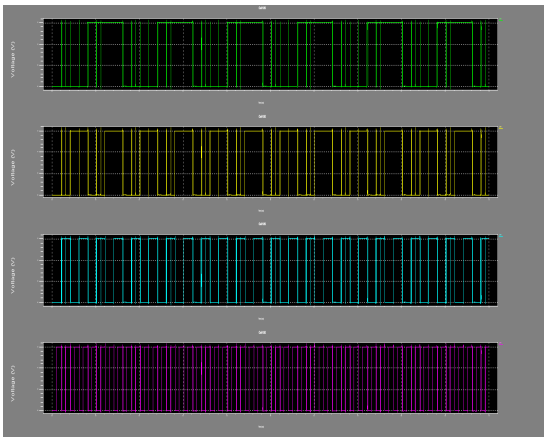

Figure 4(b). Simulation waveform of Fan et al 1 encoder at 130nm technology node

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