Approach over conventional Sequential Test approach.

7. Conclusion and Future Work

In this paper we have implemented parallel test scheduling of cores upon certain benchmark circuits having different cores configuration and placed in 3 D Stacked arrangements. The results support the improved performance of proposed methodology over conventional method. We propose to extend this scheme for testing of higher order stacked SoCs consisting of same or different benchmark circuits to study the temperature profiles of cores. We also propose to draw svg image of benchmark circuits after completing tests to study the temperature profile contours on the circuit to indicate the hottest spot generated during tests.

8. References

[1] Erik J. Marinissen, Yervant Zorian, "Challenges in Testing Core-Based System ICs", *IEEE Communication Magazine*, June 1999, pp. 104-109.
[2] P.K. Nag, A. Gattiker, S. Wei, R. D. Blanton and W. Maly, "Modelling the Economics of Testing - A DFT Prespective" *IEEE Design and Test of Computers, 10 (I):* January 2002, pp. 29-41.
[3] B. Vermeulen, C. Hora, B. Kruseman, E. J. Marinissen, R. Rijsinje, "Trends in Testing Integrated Circuits", *IEEE Test Conference, 2004. Proceedings. ITC 2004.*IEEE, 26-28 Oct 2004, pp. 688-697.
[4] Huang, W., Ghosh, S., Velusamy, S., Sankaranarayanan, K., Skadron, K. and Stan, M. R., "Hotspot: A Compact Thermal Modeling Methodology for Early-Stage VLSI Design", *In IEEE Transactions on VeryLarge Scale Integration (VLSI) Systems*, 14(5), 2000: pp 501–513.
[5] Pedram, M. and Nazarian, S.. "Thermal Modeling, Analysis and Management in VLSI circuits; Principles and Methods", *In Proc. IEEE*, vol.94, issue 8, 2006, pp 1487-1501.
[6] Yao, C., Saluja, K. K. and Ramanathan, "Test Scheduling for Circuits in Micron to Deep Submicron Technologies", *In International Conference on VLSI Design*, 2011.
[7] Zou,W., Reddy, S.M. ,. Pombenz, I. and Huang, Y., "SoC Test Scheduling using Simulated Annealing", *In Proc. IEEE VLSI Test symposium*, 2003, pp 325-330.
[8] Koranne, S.and V. Iyengar,V.," On the use of k-tuples for SoC Test Schedule representation", *In Proc. ITC* 2002 pp. 539-548.
[9]Dasilva, F., Zorian Y. et.al.," Overview of IEEE P1500 Standard", *In Proc. IEEE International Test Conference* , 2003, pp. 988-997.
[10]Early, J.," Speed, Power and Component Density in Multielement High Speed Logic System", *In Proc. IEEE International Solid State Circuits Conf.* pp. 78-79.
[11]C.R. Kime and K.K. Saluja, "Test scheduling in testable VLSI circuits", *Intl. Symposium on Fault Tolerant Computers*, 1982, pp. 406–412.
[12] H. Krawczyk and M. Kubale, " An Approximation Algorithm for Diagnostic Test scheduling in Multicomputer Systems," *IEEE Trans. on Computers*, *C-34(9):* 1985, pp. 869–872.
[13] M.S. Abadir and M.A. Breuer, " Constructing optimal test schedules for VLSI circuits having built-in test hardware," *Intl. Symposium on Fault Tolerant Computers*, 1985, pp. 165–171.
[14] W. D. Tseng, "Power –Oriented test Scheduling for SoCs," *International Journal of Computer Science and Network Security*, vol.6, no.11 November 2006.
[15]X. Wu et.al, " Test- Access Mechanism Optimization for Core-based Three Dimensional SoCs," *in Proc ICCD*, 2008, pp 212-218.
[16]Jiang et.al, "Test Architecture Design and Optimization for Three Dimensional SoCs," . *In Proc. DATE*, 2009, pp 220-225.
[17]E. J. Marinissen, " Testing TSV based Three-Dimensional Stacked ICs," *in Proc. DATE* 2010, pp. 1689-1694.
[18] Indira Rawat, M. K. Gupta, Virendra Singh, "Parallel Test Scheduling of 3 D Stacked SoCs with Temperature and Time Constraints", *IOSR-JVSP, Vol 5, Issue 4, Ver II*, Jul-Aug 2015, pp 1-13.
[19] Erik J. Marinisen, V. Iyenger and K. Chakrabarty, "A set of benchmarks for modular Testing of SoCs", *ITC,* 2002.